R&D cost improvement opportunity using quantitative benchmarking for a global semiconductor IDM

Background

Client situation
- A top-10 global semiconductor IDM
- R&D spend was higher than peers
- Management was unclear how to best address spending gap

Engagement objectives
- Identify root causes of higher R&D spend
- Prioritize “easy wins” to pursue first
- Quantify benefits of improvement initiatives

Approach

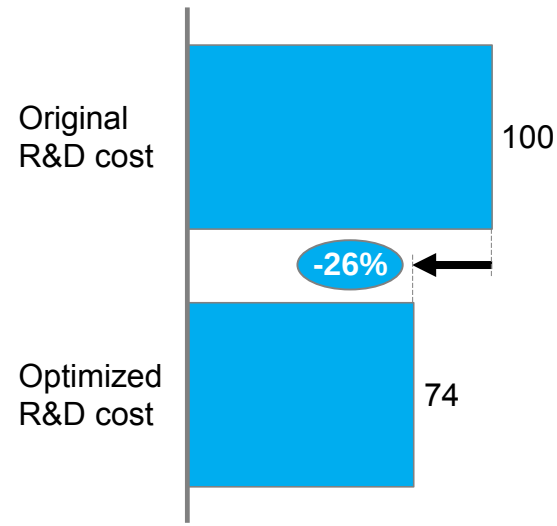
Establish capability baseline
- Measure R&D performance of teams on 3 recently completed IC development projects
- Select peers targeting same type of End Equipment Category, having similar complexity and analog content

Root-cause analysis
- Compared client’s projects to peer average and top quartile
- Normalized results based on design complexity
- Uncovered root causes of higher R&D spending

Impact

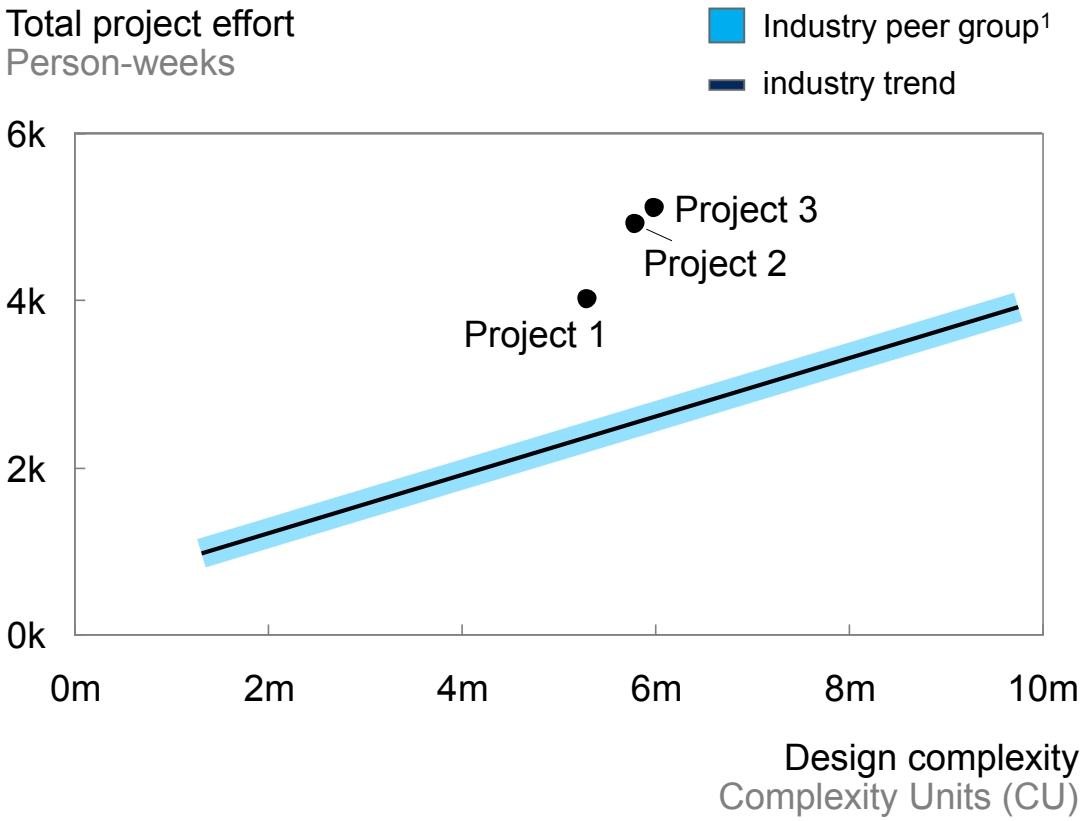
- Identified largest (26%) opportunity to reduce spending in validation
- Main issue: peers used end-to-end validation methodology while client used unit-level validation.
- Also identified opportunities in silicon respins and geographical consolidation of development

R&D Cost impact
Percent



Performance benchmarking revealed that overall "efficiency" of Client's projects was lower than peers

Development efficiency versus Design Complexity

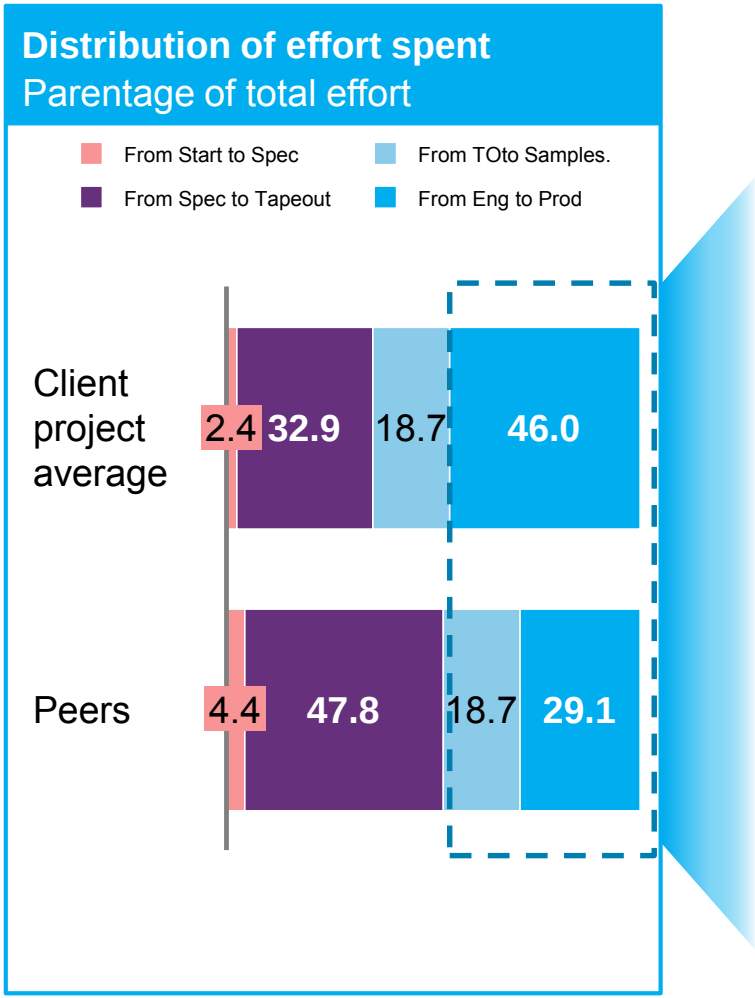


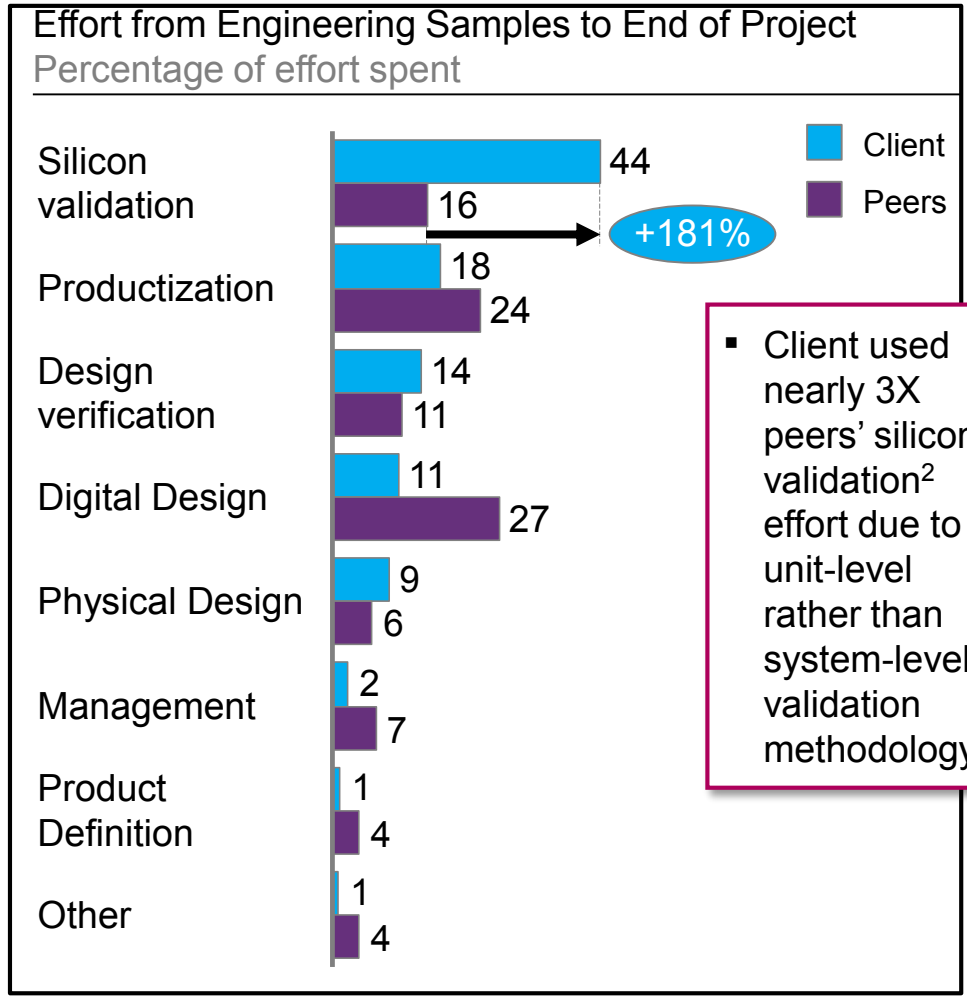
- Project effort spent on Client projects is 1500 to 2300 person-weeks higher than the peer group, for projects of equivalent complexity
- Project teams can generally process lower levels of complexity units with a given effort

1 Peer group defined based on IC's main functions, complexity levels, process technology, team sizes, percentage of analog/ mixed signal content. The light blue band highlights a 50% confidence interval over the average value for the peer group

SOURCE: First run of Numetrics analysis on Client projects

Further analysis revealed that most of the effort gap is in silicon validation



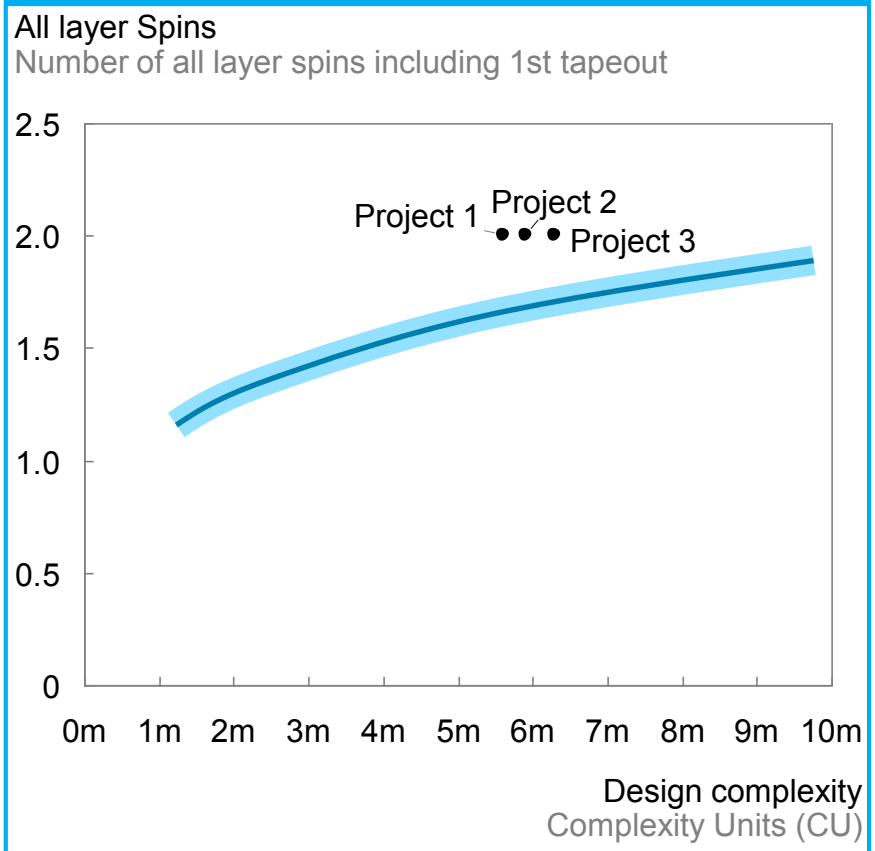


1 Taken as an average representative case of the Client project set
2 Includes all the certification, qualification, characterization, production test etc. activities

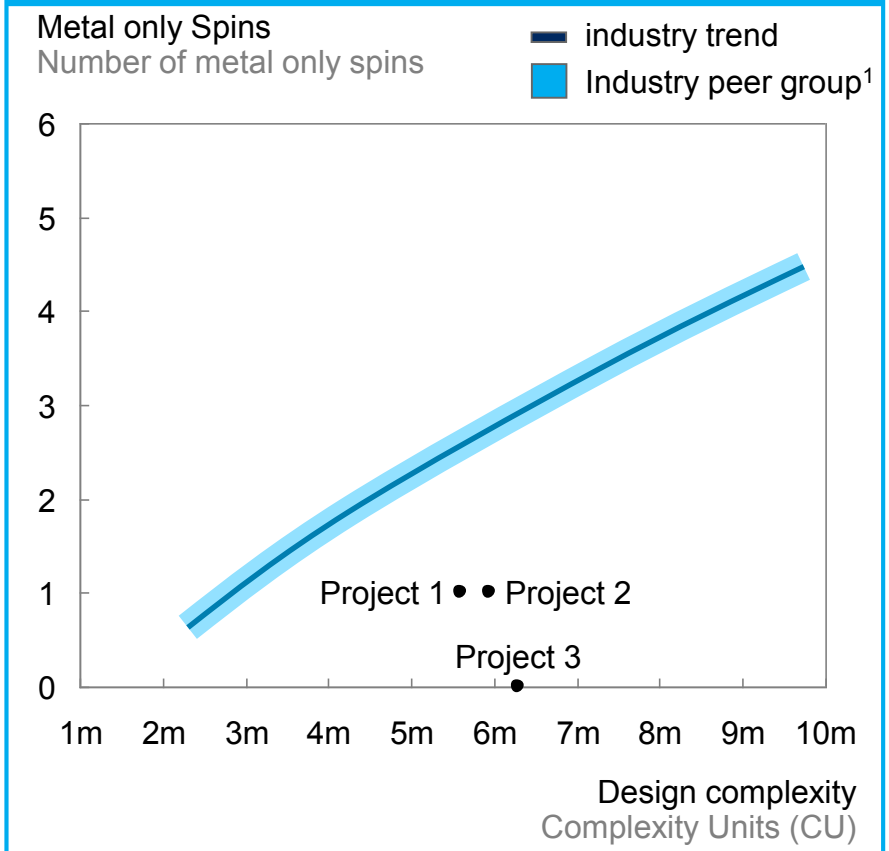
SOURCE: First run of Numetrics analysis on Client projects

Root-cause analysis showed the cause to be using more all-layer and less metal spins than peers

All layer spins against Design Complexity



Metal only spins against Design Complexity



- All-layer spins, as compared to metal ones, imply increase in cycle times and effort

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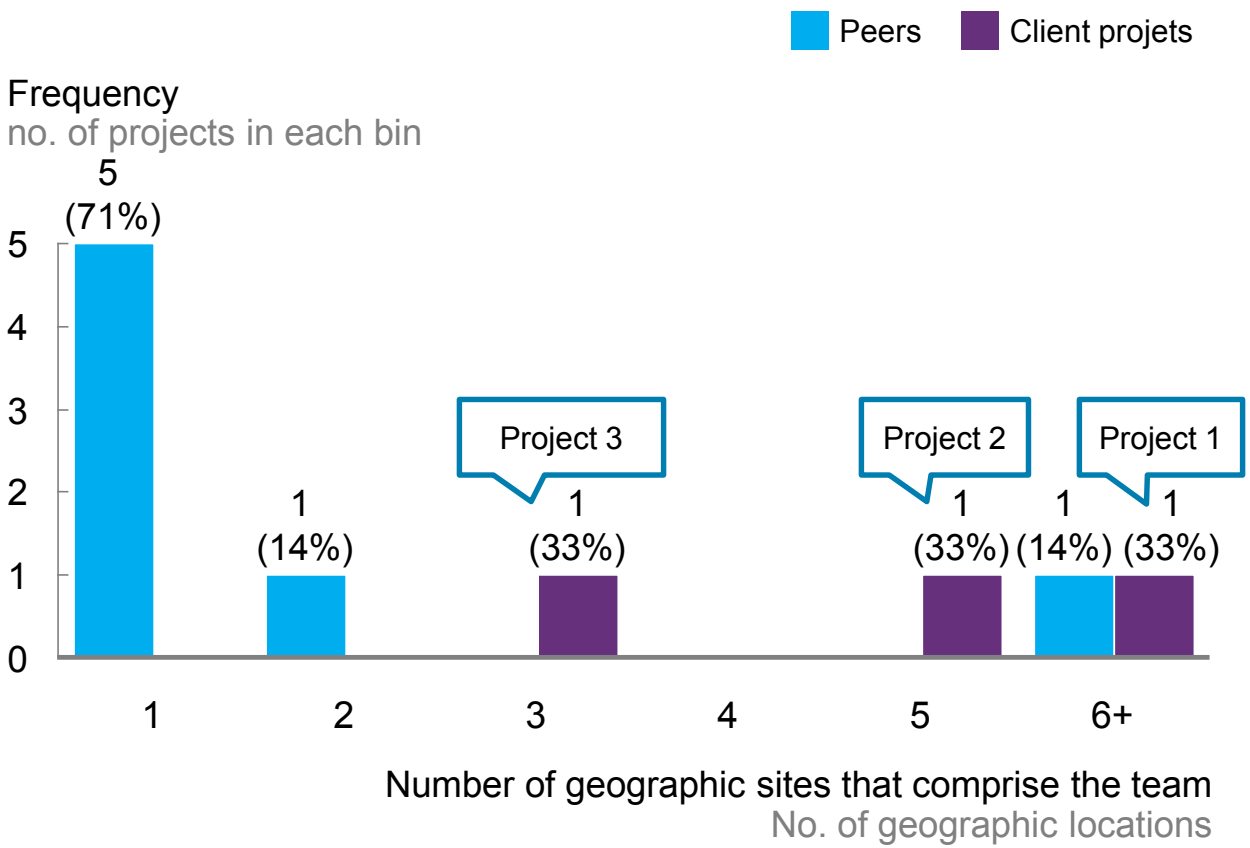
SOURCE: First run of Numetrics analysis on Client projects

Geographical distribution also impacted productivity, with projects spread across 3 more sites

Comparison of geographical distribution of project development



- Average number of development sites is 5 for Client projects, as compared to 2 for the peer group
- Within the IC HW industry, the average impact of each additional development site is a 10% productivity loss[1]

1 Benchmark obtained out of >2000 IC projects Numetrics database

SOURCE: First run of Numetrics analysis on Client projects